A MONOLITHIC GaAs DECISION CIRCUIT FOR GBIT/S PCM TRANSMISSION SYSTEMS*

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ABSTRACT

A new monolithically integrated GaAs decision circuit has been fabricated in order to satisfy speed requirements of a 840 Mbit/s coaxial cable PCM transmission system. The circuit is of SSI complexity (about 60 integrated components) and utilizes normally-on type MESFETs with 0.75-µm gate length, exhibiting a cutoff-frequency f_T = 20 GHz. The main features of the circuit performance are : high clock frequency capability (up to 3 GHz), 100-ps rise- and fall-times, high dynamic sensitivity (65 mV peak-to-peak over a 1 GHz bandwidth), and moderate power consumption (350 mW typically). The described IC is able to drive low impedance transmission lines (output signal 600 mV/50 Ω) and can be used for multilevel signal regeneration in the 1-2 Gbit/s range.

INTRODUCTION

The continuing advances in the state of gallium arsenide integrated circuits (GaAs ICs) have made possible their increasing use in ultra-high-speed analog and digital signal processing [1 - 4]. Moreover, the GaAs technology has now reached a sufficient maturity to allow the fabrication of monolithic circuits capable of performing useful electronic functions. The integrated device presented in this paper constitutes a demonstrative result of efforts carried out at Thomson-CSF since several years to develop practical purpose GaAs circuits, especially for communication applications.

It is known that digital communication systems offer various advantages over analog ones, including better performance and lower cost. However, they require a much larger bandwidth for the same capacity. Bit rates up to several hundreds of Mbit/s are needed for large capacity PCM systems suitable to carry, over coaxial cable, a number of telephone channels comparable to the most powerful FDM systems. Even using the advanced silicon technology (5 GHz - f_T bipolar transistors), performance of present-day high-speed PCM systems appears to be limited at bit rates of about 600 Mbit/s [5]. The speed limitation is mainly due to the digital regenerative repeater, and the achievement of higher bit rates requires a significant speed-performance improvement, especially for its key component, the decision circuit. It is the objective of this paper to demonstrate the capability of the GaAs ICs technology in achieving a sufficient speed to perform multilevel signal regeneration at bit rates exceeding 1 Gbit/s.

CIRCUIT DESIGN

The decision circuit (also called the regenerator) operates in the analog-digital mode by performing the following three functions :

1) Binary decision, at timing intervals defined by a sampling signal, on the status of the weakened and distorted analog signal issued from the repeater input.
2) Retiming of the incoming pulse train
3) Reshaping of the output signal according to the transmission format

The circuit described in this paper was intented for utilization within a 840 Mbit/s PCM system, with a 4B/3T (Binary/Ternary) line code leading to a symbol speed of 635 Mbaud. Due to the choice for a ternary format, the regenerative repeater must be provided with a pair of regenerator (essentially a binary device) in order to restore the 3-level transmitted signal. As shown in fig. 1, each decision circuit operates on a pair of symbols (+ 1, 0 and 0, - 1) by means of a proper threshold setting, and the ternary output train results from analog summing of the two restored binary half-signals.

Fig. 2 shows the schematic circuit diagram of the integrated regenerator. It was designed with three functional blocks which can be seen also in fig. 1 :

1) An adjustable threshold amplifier circuit (TA, including the FETs T1 to T6),
2) An edge-triggered D-type flip-flop (DFF) implemented with the popular 6-NOR gate logic diagram,
3) An interface circuit designed by using a dual-gate FET as output buffer (OB).

The so-called "Buffered-FET-Logic" (BFL) approach [1] was utilized for the DFF implementation. The main features of a similar GaAs-integrated DFF circuit were described in a previous paper [6]. Particularly, it was demonstrated that the circuit leads to a sampling action occuring at each negative transition of the clock signal, even for very short (about 300 ps) data pulses.

Various versions of threshold amplifier have been studied and compared by using both performance computation and evaluation of fabricated test circuits. The purpose of comparison was to select the circuit configuration offering the best tradeoff between the present status of our fabrication process, and the following criteria :

- a good thermal stability of the threshold voltage,
- a high enough voltage gain, ensuring a high regenerator sensitivity,
- a large frequency bandwidth, in order to optimize the propagation delay, and thus to reduce the differences of delays between signals of different waveforms,
- a circuit complexity, and a power consumption, both as low as possible.

For instance, the popular differential comparator was found to be disfavorable for the compromise between achievable transfer gain and complexity.

The circuit which has been retained (fig. 2) is issued from the BFL inverter configuration. The voltage gain is achieved by a classical common-source FET circuit with active load (FETs T_3 and T_4). However, on the contrary of the BFL logic gate, the same geometry is chosen for both transistors, so that the transfer gain is maximum when the gate of T_4 is grounded. Thus, the circuit exhibits a natural threshold (actually the ground potential), and it is the role of the first

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stage to shift the incoming signal with respect to this internal reference. In the present circuit, the threshold adjustment results from control of the current (by means of the voltage V_{Th}) drived by the common-drain FET T_1. A third stage (T_5, T_6) was finally added to allow direct coupling of the threshold amplifier output with the DFF data input. It must be emphasize that, since the TA circuit and the DFF constitutive gates exhibit a similar structure, the same supply voltages (V_{DD} = + 4 V, V_{SS} = - 4 V nominally) are required.

On the other hand, the use of a dual-gate FET as output buffer allows :

- the parallel operation of several decision circuits, and thus, the regeneration of a multilevel signal (fig. 1),
- the accurate equilibrium between the various output levels by adjustment of the upper gates bias voltage.

FABRICATION TECHNOLOGY

Main features of the material and fabrication process are followings :

- VPE active layer ($N = 1 - 1.5 \times 10^{17}$ cm^{-3}) grown on Cr-doped semi-insulating GaAs substrate with an undoped buffer,
- 6-step fabrication process including E-beam lithography, lift-off engraving, and localized etching of the channel (recessed-gate FET structure),
- dual-metal-layer interconnection system, Ti/Pt/Au gates, and integrated Ni-Cr resistors.

In order to achieve simultaneously high-speed performance, moderate power consumption, and high output-signal level, the circuits were fabricated with the following layout rules :

- submicrometer FET gate-length (typical range 0.7 - 0.8 µm) and source-drain distance of 3.6 µm,
- FET widths ranging from 15 µm to 200 µm (output buffer).

Fig. 3 shows a SEM view of the fabricated circuit. Including the bonding pads, the circuit area is 0.5 x 0.5 mm^2.

A fairly large number of wafers have been processed, with FET pinchoff voltages ranging from - 1.0 to - 1.5 V. A satisfactory fabrication yield exceeding 60 % was obtained for most wafers. Besides, a high uniformity was routinely achieved for the electrical characteristics of the circuit, as it is demonstrated by fig. 4 which shows the power consumption histogram measured for a typical wafer.

IC PERFORMANCE EVALUATION

The regenerators were encapsulated into a specially designed 10-pin flat-type package suitable for multi-gigabit data rates. In order to determine the maximum clocking frequency, the circuits were tested with a sinewave input signal whose frequency was doubled and amplified to provide the synchronous clock pulses. Fig. 5 illustrates the very efficient reshaping so achieved at 1 GHz clock frequency. A correct signal regeneration up to a clocking frequency of 3 GHz was measured for the fastest circuits. A 2 GHz toggle performance is routinely performed without chip selection.

The rise- and fall-times measured in a 50Ω test fixture exhibit a comparable value of about 100 ps (20-80 %). Under the realistic assumption that these transition times cannot exceed 1/10 of the signal period duration, a maximum clock frequency of about 2 GHz is deduced for PCM system applications.

The dynamic sensitivity is an important parameter defined as the smallest noise-free signal at half clock frequency for which an error-free decision can be taken at optimum settling of the threshold. In fig. 6, the measured sensitivity is plotted as a function of the clocking frequency. A flat sensitivity (3 dB) is achieved up to 1 GHz with a value of 65 mV peak-to-peak. At 2 GHz, the dynamic sensitivity was still 220 mV. This parameter is mainly determined by the gain-frequency relationship of the threshold amplifier. The present circuit exhibits a gain of 13 dB with a cutoff frequency of 1.6 GHz.

Other parameters of practical interest have been measured at 1 GHz clock signal : the propagation delay time between clock and output t_{pd} (C, S), the set-up time t_{su}, and the hold-time t_h. In addition to the maximum clock frequency, f_c^{max}, the knowledge of these times allows to deduce the BFL-NOR-gate propagation delay time t_{pd} (FI/FO = 1/1) as well as its fan-out sensitivity. The results obtained in this way, summarized in Table I, agree well with the more accurate ring-oscillator performance measurements [6].

Table 1 - Experimental speed-performance of the decision circuit

f_c^{max}	t_{pd}(C,S)	$t_h + t_{su}$	t_{pd}(1/1)	Δt_{pd}/FO
3 GHz	310 ps	205 ps	69 ps	18 ps

It must be emphasized that the output buffer contributes greatly to increase the intrinsic delay time (135 ps in the present case), due to the large width (200 µm) of the dual-gate FET heavily loading the flip-flop output. Conversely, a high output swing of 600 mV peak-to-peak/50 Ω is achieved.

The circuit of table I exhibits a power consumption of about 350 mW, with 83 mW for TA, 237 mW for DFF, and 32 mW for the output interface. The IC was tested within the temperature range 0-70°C and a fairly good stability (a threshold drift below 50 mV) was observed with no compensation circuit.

It was found that the FET transition frequency, $f_T = g_m/2\pi C_{gs}$, appears to be a good figure of merit for the empirical relationship between transistors and IC performances. Thus, it was concluded from experience that the DFF toggle frequencies roughly vary like f_T, for given processing technology and design rules. This conclusion was confirmed by measuring the small signal equivalent circuit (fig. 7) of a test transistor fabricated simultaneously with each processed wafer. The analysis procedure requires measurement of both S-parameters in the 4-10 GHz range and parasitic resistances at low frequency, and subsequent fit of the circuit elements by computer program. Table II illustrates the result of this analysis for the circuit of table I (test transistor geometry : L = 0.75 µm, Z = 200 µm)

Table II - Circuit parameters for an integrated GaAs-MESFET

g_{mo} = 32 m℧	C_{gs} = 0.26 pF	τ = 11 ps
R_i = 31 Ω	g_{ds} = 1.3 m℧	C_{gd} = 0.037pF
C_{ds} = 0.08 pF	R_g = 27 Ω	$R_s = R_d$ = 11 Ω

A transition frequency f_T = 19.6 GHz is deduced for this particular circuit.

CONCLUSIONS

The regeneration of 3-level signals was tested by using a pair of decision circuits, accordingly to the diagram of fig. 1. Fig. 8 illustrates the signal before and after regeneration at 560 Mbit/s ; for this experiment, the incoming ternary sequence was generated by means of commercialy available devices. Furthermore, in fig. 9 is shown a typical 3-level eye pattern observed at the dual-regenerator output at 1 GHz clock frequency. These results appear to be quite excellent and hold great promise for utilization in PCM systems at higher bit rates (in the 1 - 2 Gbit/s range) or for extension towards other ultra-high-speed analog applications (for flash-AD-conversion, for instance).

ACKNOWLEDGMENTS

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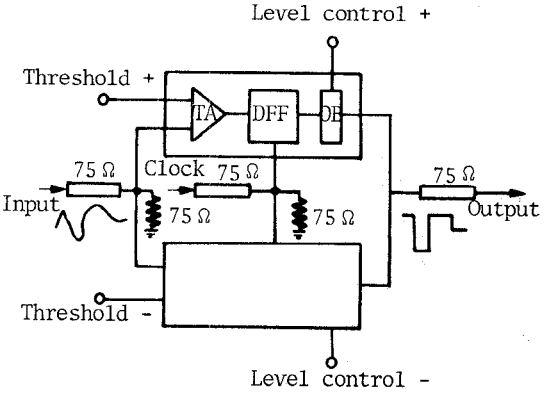

Fig. 1 - Block diagram of a 3-level regeneration circuit using a pair of regenerators.

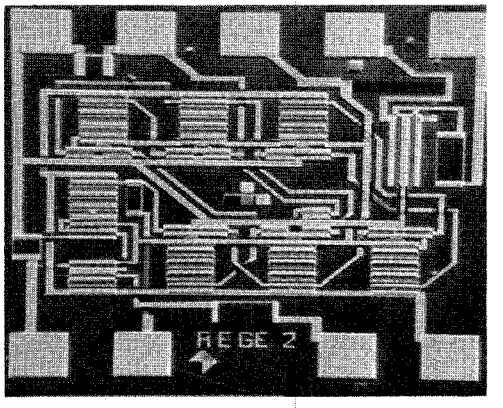

Fig. 3 - SEM microphotograph of the decision circuit (area : 0.5 x 0.5 mm²)

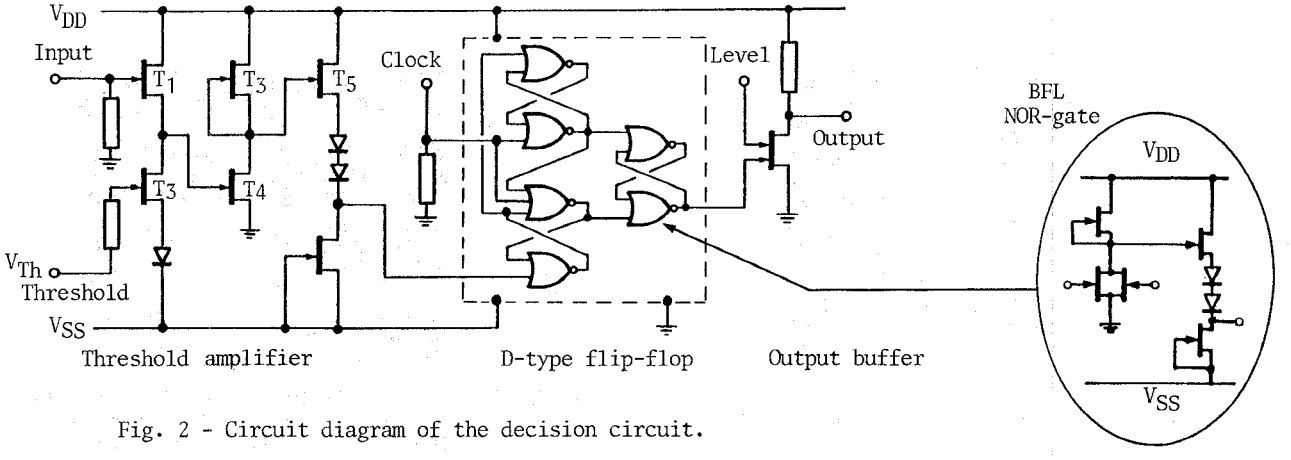

Fig. 2 - Circuit diagram of the decision circuit.

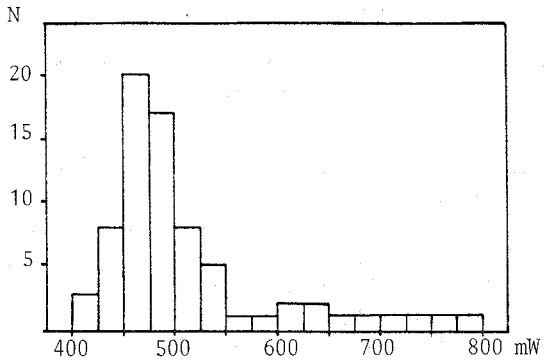

Fig. 4 - Power consumption histogram for a typical wafer.

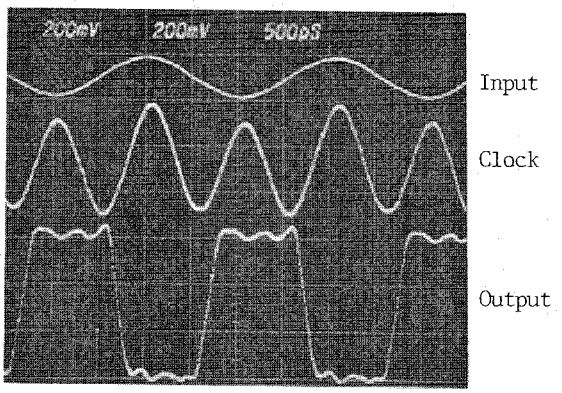

Fig. 5 - Sinewave signal regeneration at 1 GHz clock frequency (horizontal scale : 500 ps/div - vertical scales : 200 mV/div)

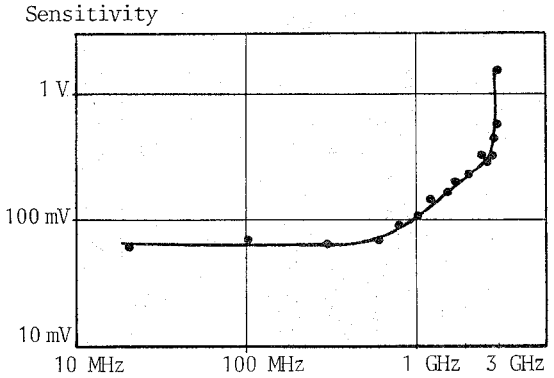

Fig. 6 - Dynamic sensitivity (peak-to-peak) versus clock frequency.

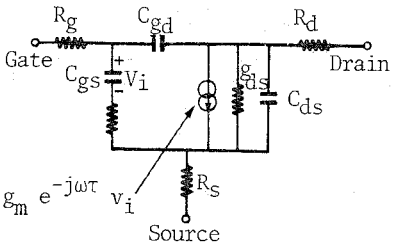

Fig. 7 - Small signal FET equivalent circuit.

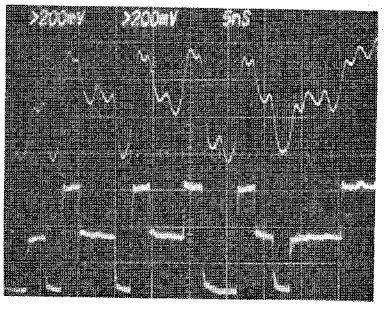

Fig. 8 - 560 Mbit/s three level signal operation waveform before and after regeneration

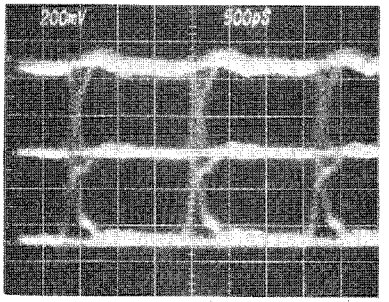

Fig. 9 - 3-level eye pattern at the regenerator output for 1 GHz clock frequency (horizontal scale : 500 ps/div)